LDO Regulator – 1 A, Ultra Low Dropout, CMOS, with Bias Rail

T30LMPSR131

The T30LMPSR131 is a 1 A LDO equipped with an NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The T30LMPSR131 offers ultra-fast dynamic response and provides very stable output voltage with 1% accuracy over full temperature range. To optimize performance for battery operated portable applications, the T30LMPSR131 features an ultra-low bias current consumption. The device also features high PSRR across frequency range and ultra-low noise optimized for noise sensitive applications. The WLCSP6 1.145 mm x 0.75 mm, 0.4 mm pitch Chip Scale package is optimized for use in space constrained applications.

Features

- Best-in-Class Dropout: 25 mV (Typ.) at 1 A
- ±1% Accuracy over −40 °C to 125 °C Temperature Range
- Ultra Low Bias Input Current of Typ. 85 μA
- Low Noise, 7.5 μV_{RMS} Typ.
- High PSRR across Frequency Range
  - 78 dB at 1 kHz
  - 40 dB at 100 kHz
- Input Voltage Range: up to 2.2 V
- Bias Voltage Range: up to 3.6 V
- Output Voltage Range: 0.5 V to 1.8 V (Fixed), Resolution 25 mV
- Excellent Load Transient Performance
- 1.2 V Logic Level Enable Input Compatibility
- Normal and Slow Turn-On Options Available
- Output Active Discharge Option Available

Typical Applications

- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

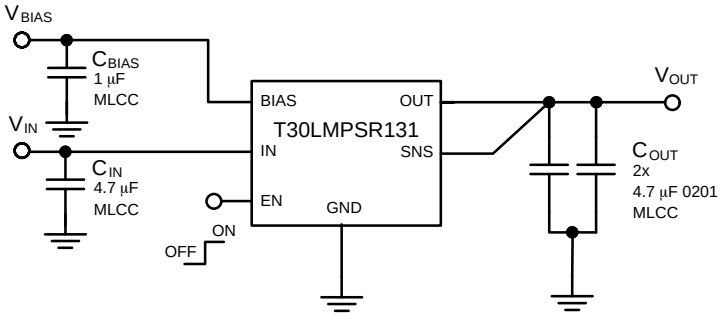
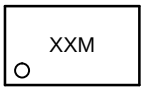


Figure 1. Application Schematic

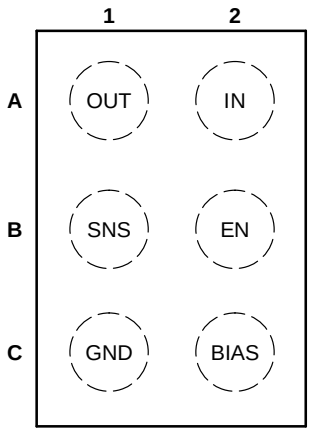
WLCSP6
1.145x0.75x0.33
CASE 567YX

MARKING DIAGRAM



XX = Specific Device Code
M = Month Code

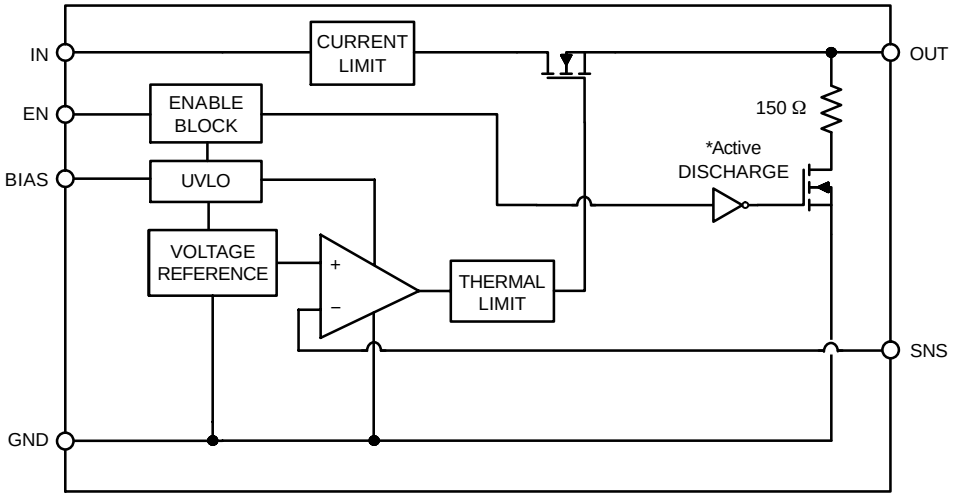
PIN CONNECTIONS



Top View

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.



*Active output discharge function is present only in “A” and “C” option devices.

Figure 2. Simplified Schematic Block Diagram - Fixed Version

PIN FUNCTION DESCRIPTION

Pin No. WLCSP6	Pin Name	Description
A1	OUT	Regulated Output Voltage pin
A2	IN	Input Voltage Supply pin. This pin is monitored by internal Under-Voltage Lockout Circuit.
B1	SNS	Output voltage Sensing Input. Connect to Output on the PCB to output the voltage corresponding to the part version.
B2	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
C1	GND	Ground pin
C2	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 2.5	V
Output Voltage	V_{OUT}	−0.3 to (V_{IN} + 0.3) ≤ 2.5	V
Chip Enable, Bias and SNS Input	V_{EN}, V_{BIAS}, V_{SNS}	−0.3 to 4.0	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device’s lifespan or reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22-A114
   ESD Charged Device Model tested per JS-002-2018
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP6 1.145 mm x 0.75 mm Thermal Resistance, Junction-to-Air (Note 3)	$R_{\theta JA}$	69	°C/W

3. This junction-to-ambient thermal resistance under natural convection was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high_K (2s2p) 80 mm x 80 mm multilayer board with 1-ounce internal planes and 2-ounce copper on top and bottom. Top copper layer has a dedicated 1.6 mm2 copper area.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	–	2.2	V
V_{BIAS}	Bias Voltage	2.5 or $V_{OUT(NOM)}$ + V_{DO_MAX} +1.5 whichever is greater	3.6	V
V_{EN}, V_{SNS}	EN, SNS Voltage	–	3.6	V
C_{IN}	Input Capacitance (Note 4)	2.2	–	μF
C_{OUT}	Output Capacitance (Note 4)	2.2	47	μF
C_{BIAS}	Bias Capacitance (Note 4)	0.47		μF
T_J	Operating Junction Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. The specified value refers to the effective capacitance, accounting for all relevant derating factors, including DC bias, temperature, and capacitor tolerance.

ELECTRICAL CHARACTERISTICS

(−40 °C ≤ T_J ≤ 125 °C; V_{BIAS} = 2.7 V or (V_{OUT} + 1.5 V), whichever is greater, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 μF, C_{OUT} = 10 μF, C_{BIAS} = 1 μF, unless otherwise noted.
Typical values are at T_J = +25 °C. Min/Max values are for −40 °C ≤ T_J ≤ 125 °C unless otherwise noted. (Note 5))

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range		V_{IN}	V_{OUT} + V_{DO}		2.2	V
Operating Bias Voltage Range		V_{BIAS}	(V_{OUT} + 1.50) ≥ 2.5		3.6	V
Undervoltage Lock-out	V_{BIAS} Rising Hysteresis	$UVLO_{(BIAS)}$		2.1 0.1		V
	V_{IN} Rising Hysteresis	$UVLO_{(IN)}$		0.8 x V_{OUT} 0.1		V
Output Voltage Accuracy	−40 °C ≤ T_J ≤ 85 °C, $V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.5 V), whichever is greater < V_{BIAS} ≤ 3.3 V, 1 mA < I_{OUT} < 1 A	V_{OUT}	−0.8		+0.8	%
Output Voltage Accuracy	−40 °C ≤ T_J ≤ 125 °C, $V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.5 V), whichever is greater < V_{BIAS} ≤ 3.3 V, 1 mA < I_{OUT} < 1 A		−1.0		+1.0	%
V_{IN} Line Regulation	$V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ 2.2 V	$Line_{Reg}$		0.01		%/V
V_{BIAS} Line Regulation	2.7 V or ($V_{OUT(NOM)}$ + 1.5 V), whichever is greater < V_{BIAS} ≤ 3.3 V	$Line_{Reg}$		0.01		%/V
Load Regulation	I_{OUT} = 1 mA to 1 A	$Load_{Reg}$		1		mV
V_{IN} Dropout Voltage	I_{OUT} = 1 A (Note 6)	V_{DO}		25	50	mV
V_{BIAS} Dropout Voltage	I_{OUT} = 1 A, V_{IN} = V_{BIAS} (Notes 6, 7)	V_{DO}		1.1	1.5	V
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$	I_{CL}	1250	1650	2000	mA
SNS Pin Operating Current		I_{SNS}		0.1	0.5	μA

ELECTRICAL CHARACTERISTICS (continued)
($-40\ ^\circ C \le T_J \le 125\ ^\circ C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.5 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.1 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 μF, C_{OUT} = 10 μF, C_{BIAS} = 1 μF, unless otherwise noted.
Typical values are at $T_J = +25\ ^\circ C$. Min/Max values are for $-40\ ^\circ C \le T_J \le 125\ ^\circ C$ unless otherwise noted. (Note 5))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Bias Pin Quiescent Current	V_{BIAS} = 3.3 V, I_{OUT} = 0 mA		I_{BIASQ}		85	130	μA
Bias Pin Disable Current	$V_{EN} \le 0.325$ V		$I_{BIAS(DIS)}$		0.5		μA
Input Pin Disable Current			$I_{VIN(DIS)}$		0.5		μA
EN Pin Threshold Voltage	EN Input Voltage “H”		$V_{EN(H)}$	0.77			V
	EN Input Voltage “L”		$V_{EN(L)}$			0.325	
EN Pull Down Current	V_{EN} = 3.3 V		I_{EN}		0.3	1	μA
Power Supply Rejection Ratio	V_{IN} to V_{OUT}, $V_{IN} = V_{OUT}$ + 0.1 V, I_{OUT} = 450 mA, C_{OUT} = 2 x 4.7 μF 0201	f = 100 Hz	PSRR(V_{IN})		73		dB
		f = 1 kHz			78		
		f = 10 kHz			58		
		f = 100 kHz			40		
	V_{BIAS} to V_{OUT}, $V_{IN} = V_{OUT}$ + 0.1 V	f = 1 kHz	PSRR(V_{BIAS})		88		dB
Output Noise Voltage	$V_{IN} = V_{OUT}$ + 0.1 V, f = 10 Hz to 100 kHz	I_{OUT} = 10 mA	V_N		10		μV_{RMS}
		I_{OUT} = 1 A			7.5		
Thermal Shutdown Threshold	Temperature increasing				160		°C
	Temperature decreasing				140		
Output Discharge Pull-Down	$V_{EN} \le 0.325$ V, V_{OUT} = 0.5 V, Active Discharge Version Only		R_{DISCH}		150		Ω
Delay Time	From assertion of V_{EN} to output voltage increase	“A” option	t_{DELAY}		120		μs
		“C” option			120		
Rise Time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	“A” option	t_{RISE}		20		
		“C” option			100		
Turn-On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	“A” option	t_{ON}		140		
		“C” option			220		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25\ ^\circ C$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
6. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
7. For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

TYPICAL CHARACTERISTICS

(Conditions: V_{IN} = V_{OUT} + 100 mV, V_{BIAS} = V_{OUT} + 1.5 V, V_{EN} = V_{IN}, C_{IN} = 4.7 μF 0201 MLCC, C_{OUT} = 2x 4.7 μF 0201 MLCC, C_{BIAS} = 1 μF 0201 MLCC, unless otherwise noted)

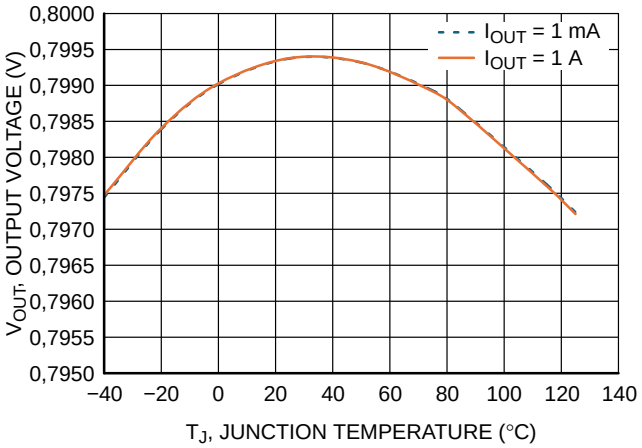


Figure 3. Output Voltage vs. Temperature − V_{OUT} = 0.8 V

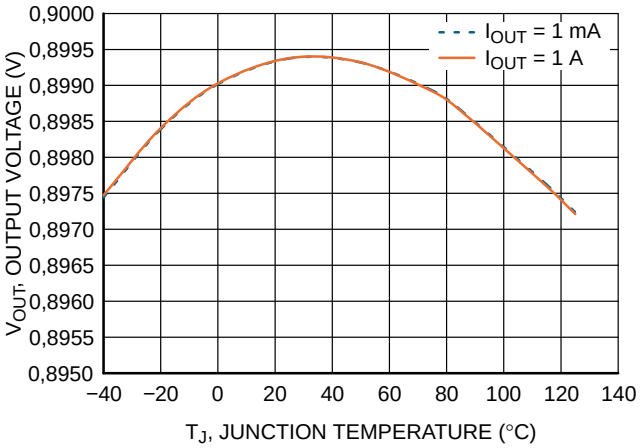


Figure 4. Output Voltage vs. Temperature − V_{OUT} = 0.9 V

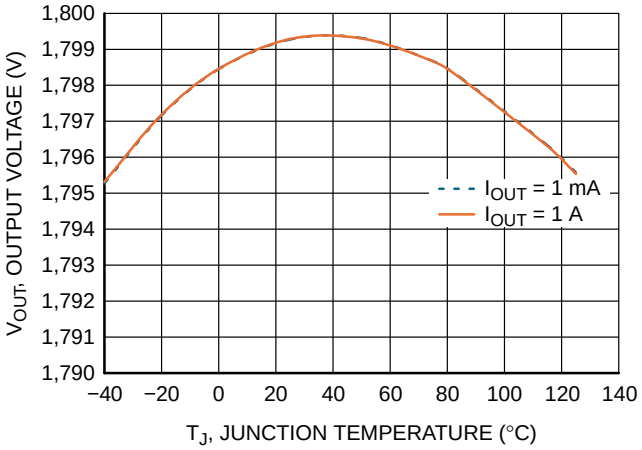


Figure 5. Output Voltage vs. Temperature − V_{OUT} = 1.8 V

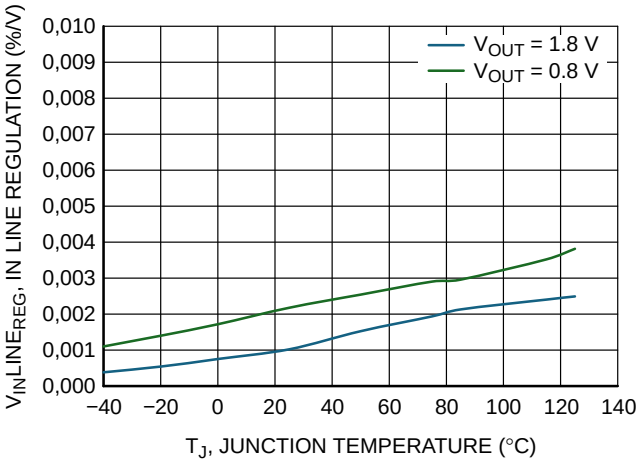


Figure 6. V_{IN} Line Regulation vs. Temperature

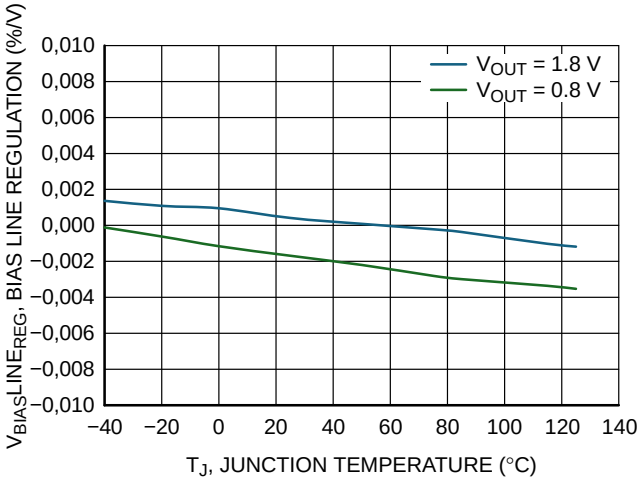


Figure 7. V_{BIAS} Line Regulation vs. Temperature

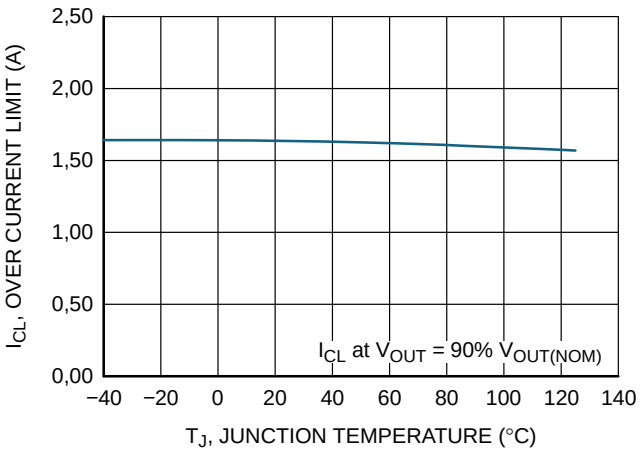


Figure 8. Current Limit vs. Temperature

TYPICAL CHARACTERISTICS

(Conditions: V_{IN} = V_{OUT} + 100 mV, V_{BIAS} = V_{OUT} + 1.5 V, V_{EN} = V_{IN}, C_{IN} = 4.7 μF 0201 MLCC, C_{OUT} = 2x 4.7 μF 0201 MLCC, C_{BIAS} = 1 μF 0201 MLCC, unless otherwise noted)

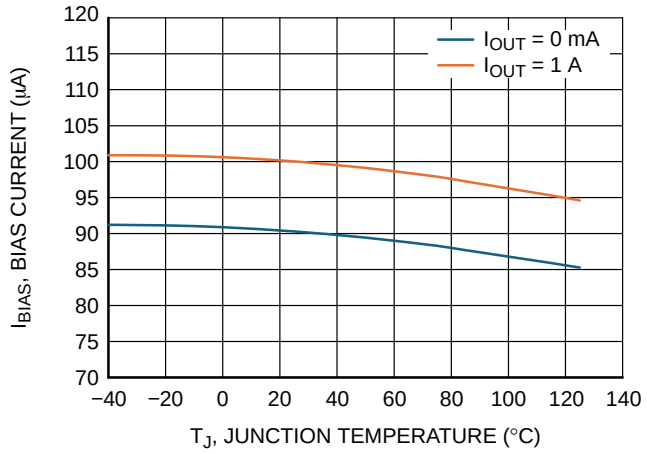


Figure 9. BIAS Current vs. Temperature

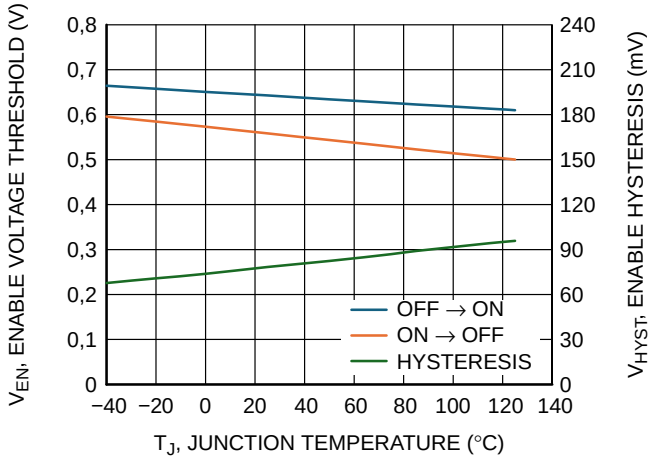


Figure 10. Enable Thresholds vs. Temperature

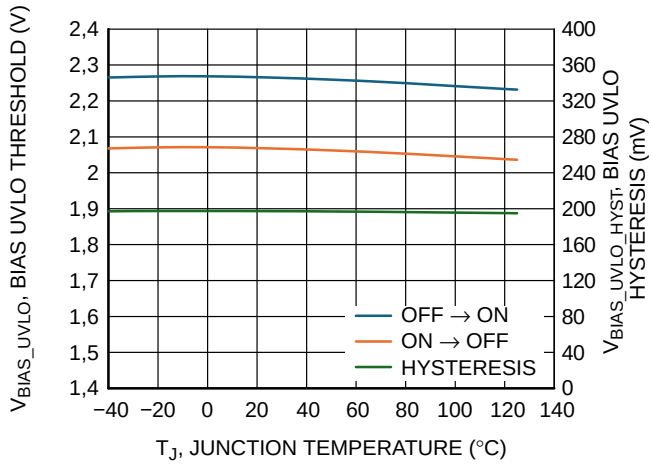


Figure 11. BIAS UVLO Thresholds vs. Temperature

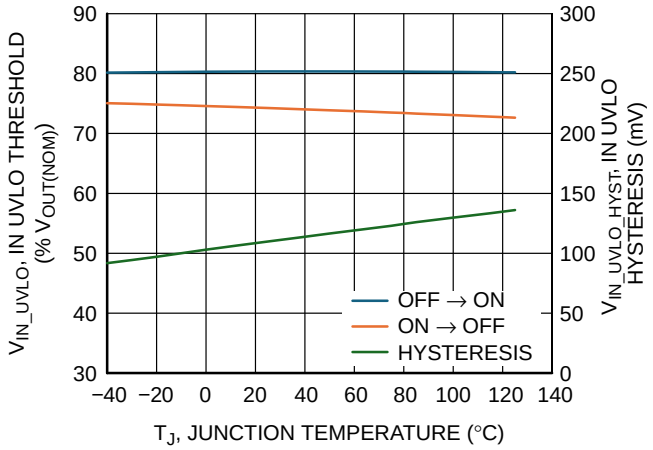


Figure 12. IN UVLO Thresholds vs. Temperature

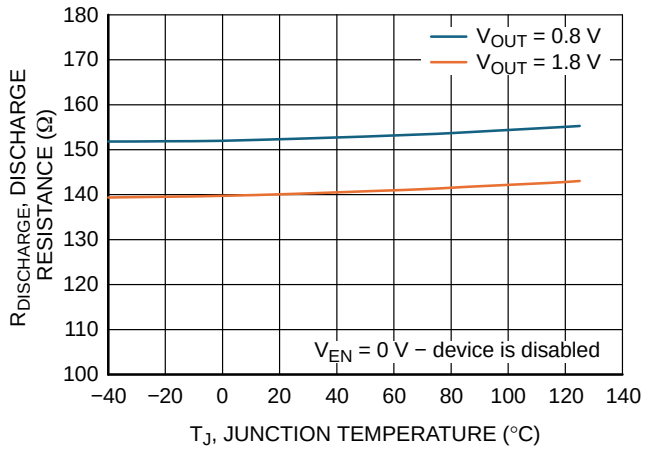


Figure 13. Active Discharge Resistance

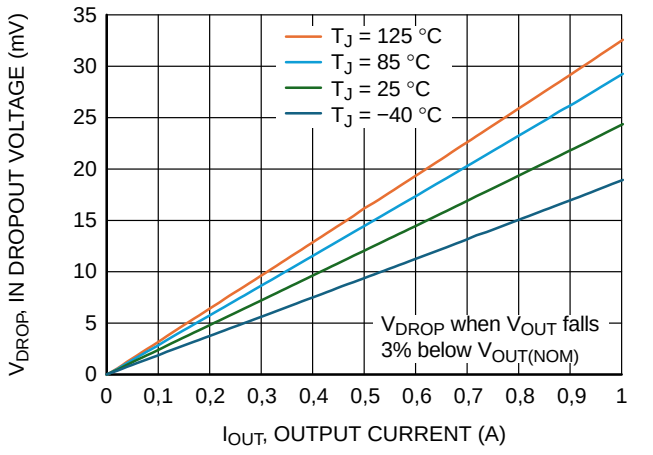


Figure 14. V_{IN} Dropout Voltage vs. Output Current

TYPICAL CHARACTERISTICS

(Conditions: V_{IN} = V_{OUT} + 100 mV, V_{BIAS} = V_{OUT} + 1.5 V, V_{EN} = V_{IN}, C_{IN} = 4.7 μF 0201 MLCC, C_{OUT} = 2x 4.7 μF 0201 MLCC, C_{BIAS} = 1 μF 0201 MLCC, unless otherwise noted)

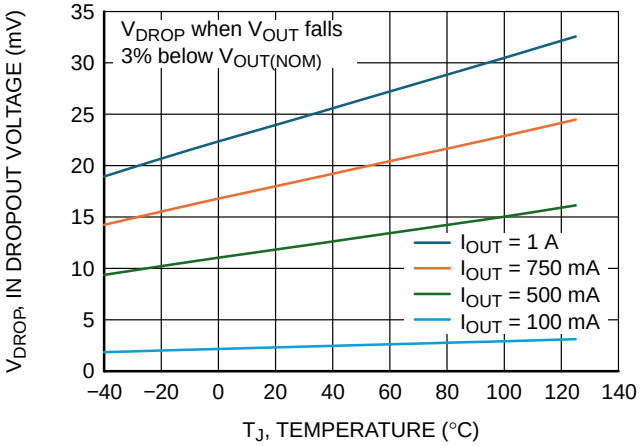


Figure 15. V_{IN} Dropout Voltage vs. Temperature

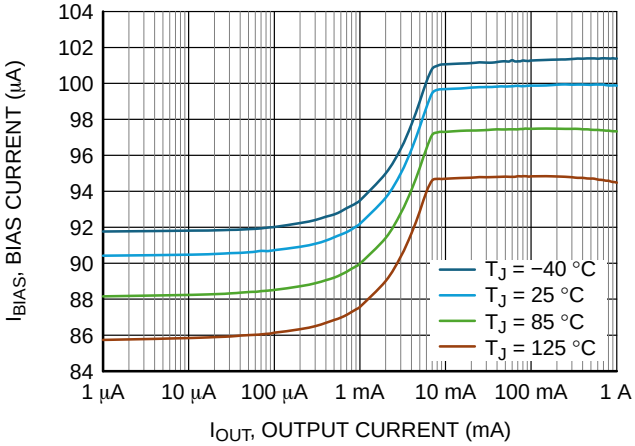


Figure 16. Bias Current vs. Output Current

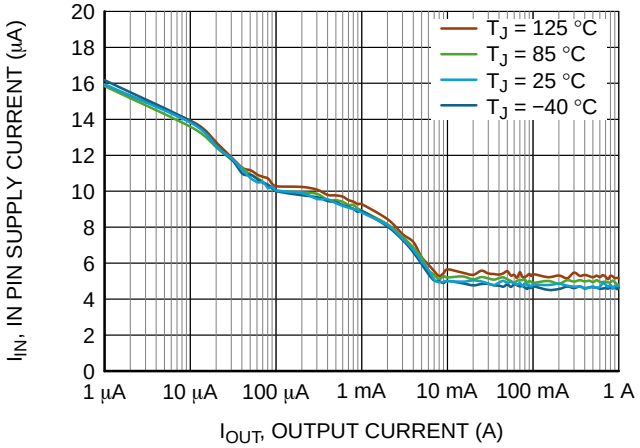


Figure 17. IN Supply Current vs. Output Current

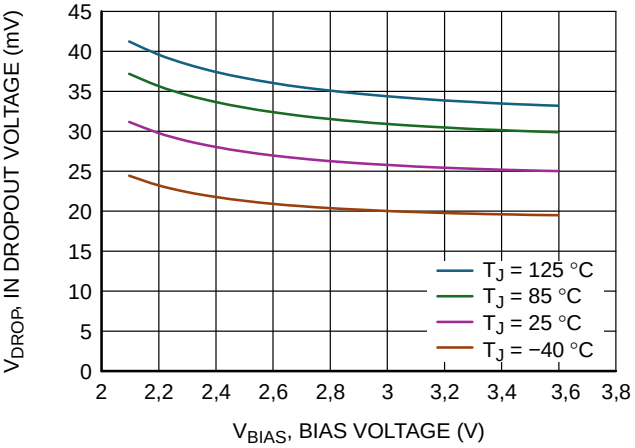


Figure 18. V_{IN} Dropout Voltage vs. BIAS Voltage

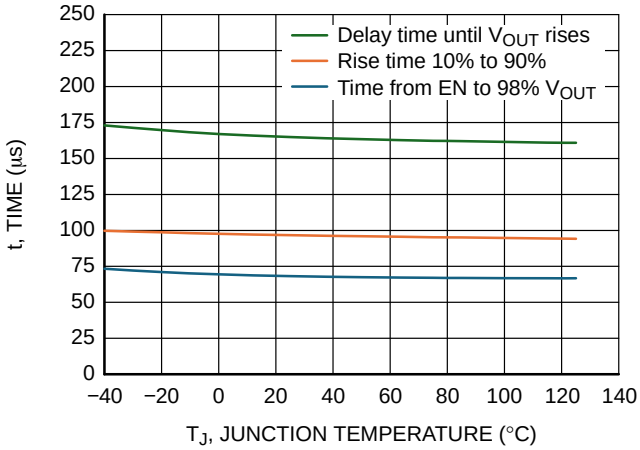


Figure 19. Soft-start Timing: EN Delay, Rise Time, and Startup Duration

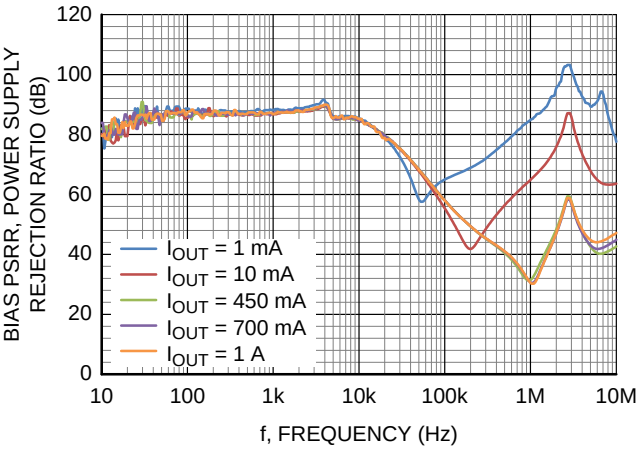


Figure 20. BIAS Power Supply Rejection Ratio − 100 mV Headroom

TYPICAL CHARACTERISTICS

(Conditions: V_{IN} = V_{OUT} + 100 mV, V_{BIAS} = V_{OUT} + 1.5 V, V_{EN} = V_{IN}, C_{IN} = 4.7 μF 0201 MLCC, C_{OUT} = 2x 4.7 μF 0201 MLCC, C_{BIAS} = 1 μF 0201 MLCC, unless otherwise noted)

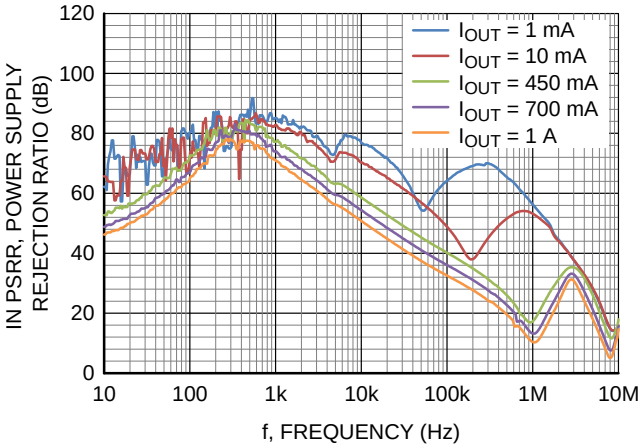


Figure 21. IN Power Supply Rejection Ratio − 100 mV Headroom

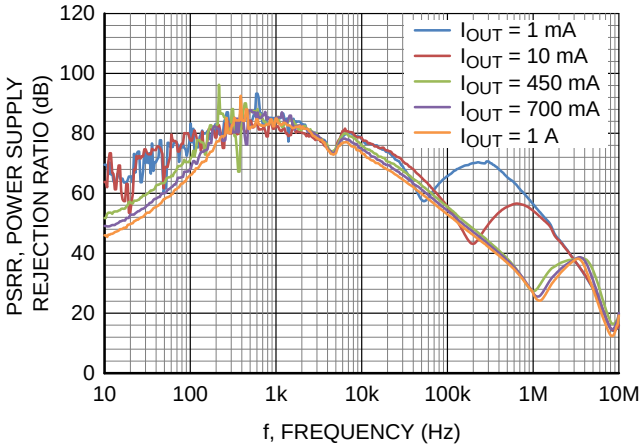


Figure 22. IN Power Supply Rejection Ratio − 300 mV Headroom

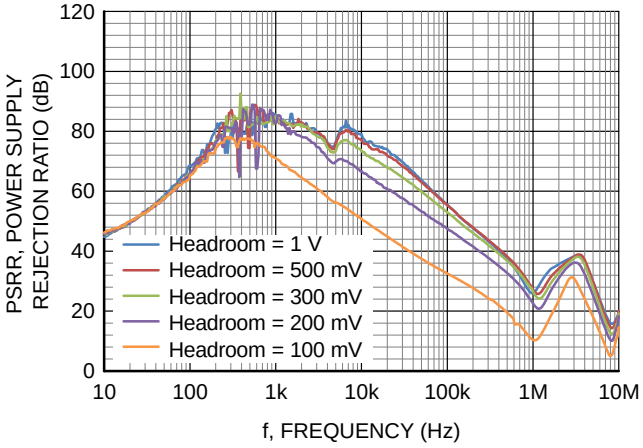


Figure 23. IN Power Supply Rejection Ratio vs. Headroom − I_{OUT} = 1 A

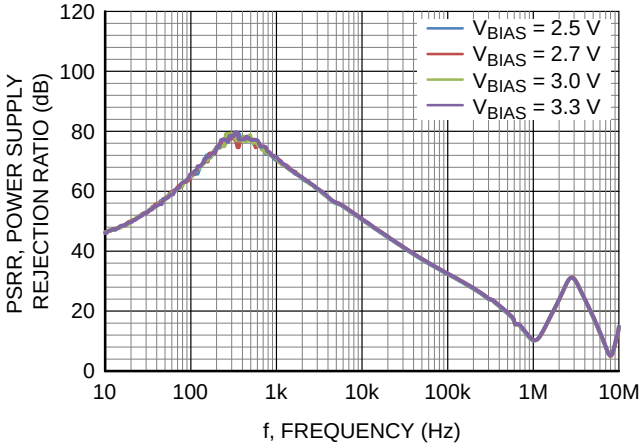
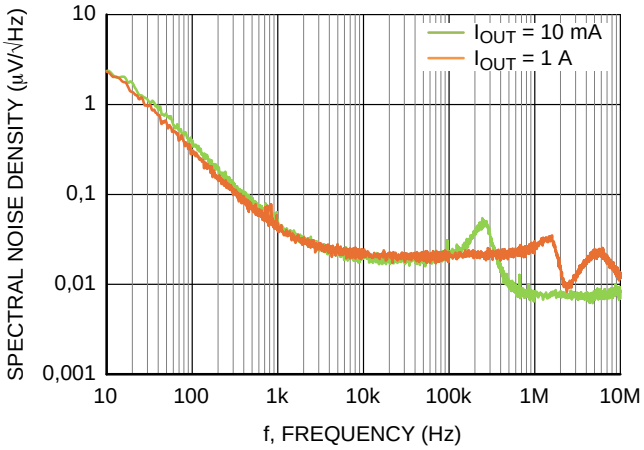


Figure 24. IN Power Supply Rejection Ratio vs. BIAS Voltage − I_{OUT} = 1 A

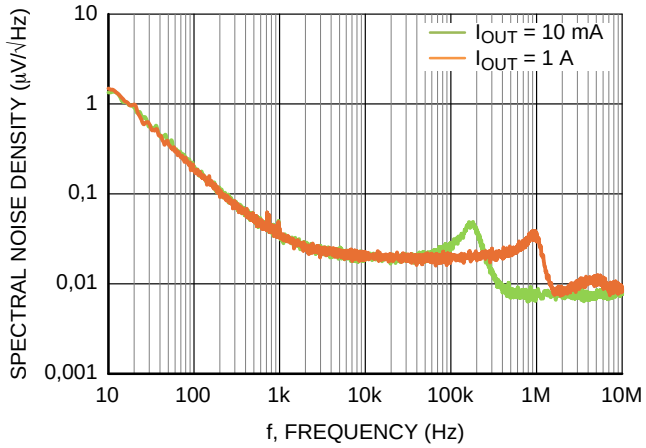


I_{OUT}	RMS Output Noise (μV_{RMS})	
	10 Hz − 100 kHz	100 Hz − 100 kHz
10 mA	8.9	7.2
1 A	8.4	6.6

Figure 25. Output Voltage Noise Spectral Density − V_{OUT} = 0.8 V

TYPICAL CHARACTERISTICS

(Conditions: V_{IN} = V_{OUT} + 100 mV, V_{BIAS} = V_{OUT} + 1.5 V, V_{EN} = V_{IN}, C_{IN} = 4.7 μF 0201 MLCC, C_{OUT} = 2x 4.7 μF 0201 MLCC, C_{BIAS} = 1 μF 0201 MLCC, unless otherwise noted)



I_{OUT}	RMS Output Noise (μV_{RMS})	
	10 Hz − 100 kHz	100 Hz − 100 kHz
10 mA	12.0	7.2
1 A	11.1	6.6

Figure 26. Output Voltage Noise Spectral Density − V_{OUT} = 1.8 V

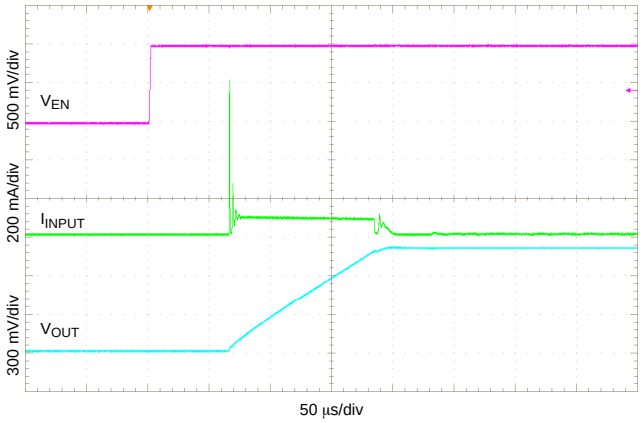


Figure 27. Enable Turn-on Response − I_{OUT} = 1 mA − "C" Option

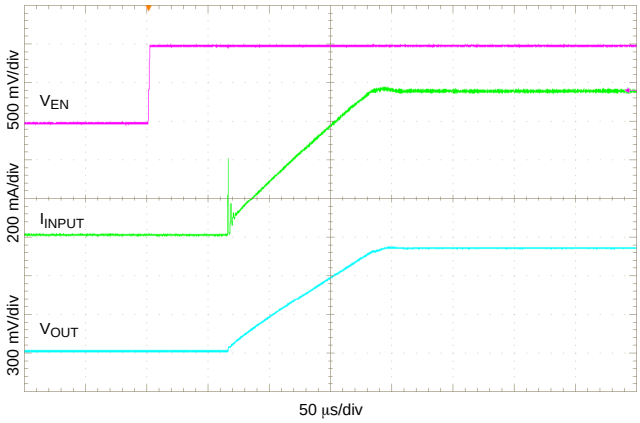


Figure 28. Enable Turn-on Response − I_{OUT} = 1 A − "C" Option

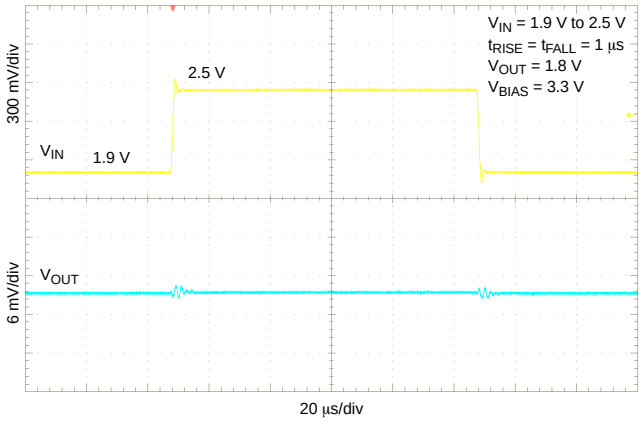


Figure 29. IN Line Transient Response − I_{OUT} = 1 mA

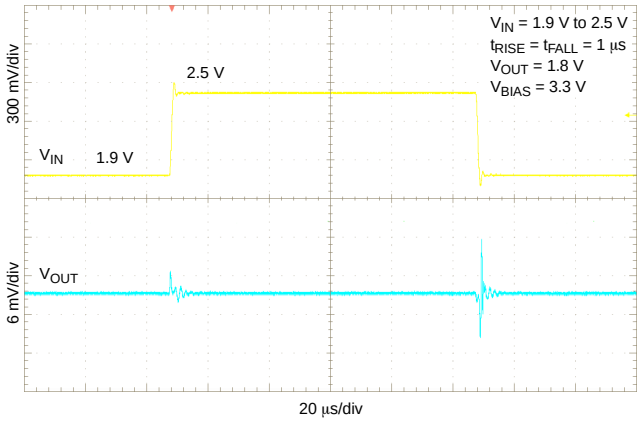


Figure 30. IN Line Transient Response − I_{OUT} = 1 A

TYPICAL CHARACTERISTICS

(Conditions: V_{IN} = V_{OUT} + 100 mV, V_{BIAS} = V_{OUT} + 1.5 V, V_{EN} = V_{IN}, C_{IN} = 4.7 μF 0201 MLCC, C_{OUT} = 2x 4.7 μF 0201 MLCC, C_{BIAS} = 1 μF 0201 MLCC, unless otherwise noted)

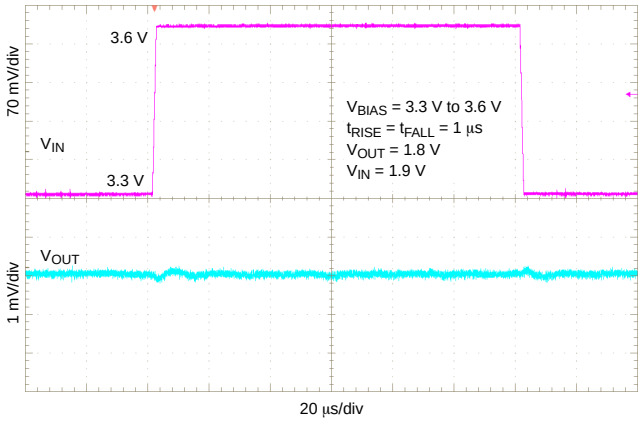


Figure 31. BIAS Line Transient Response − I_{OUT} = 1 mA

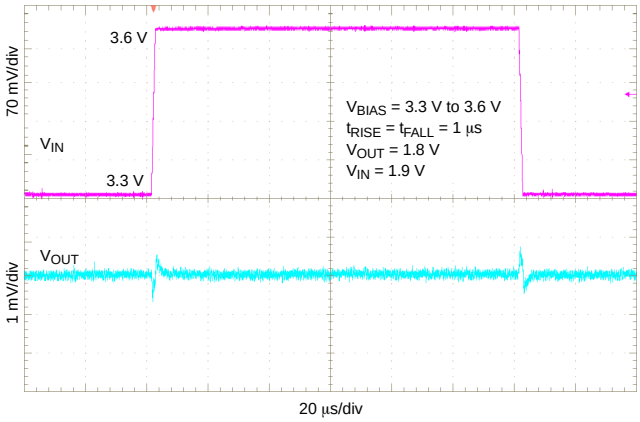


Figure 32. BIAS Line Transient Response − I_{OUT} = 1 A

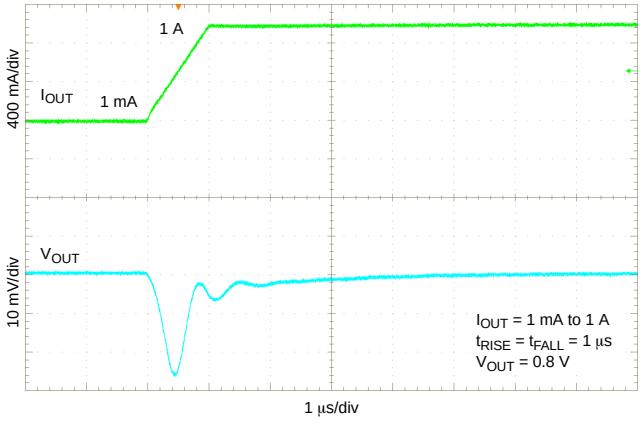


Figure 33. Load Transient Response − 1 mA to 1 A/1 μs

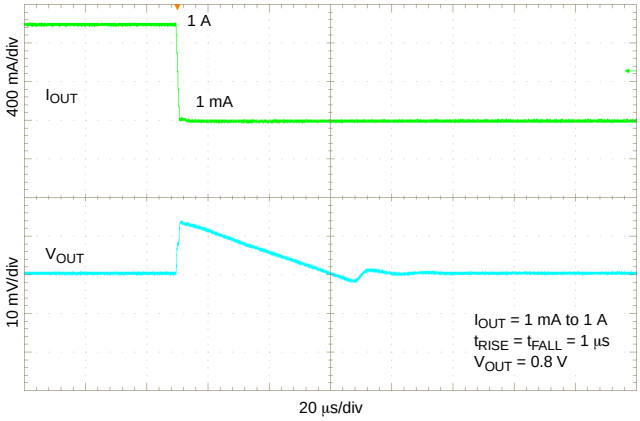


Figure 34. Load Transient Response − 1 A to 1 mA/1 μs

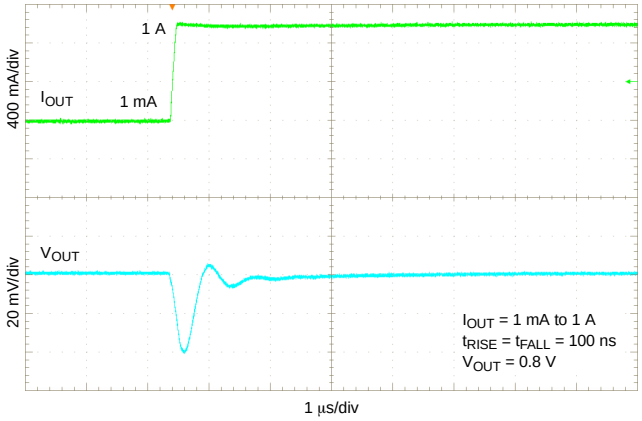


Figure 35. Load Transient Response − 1 mA to 1 A/100 ns

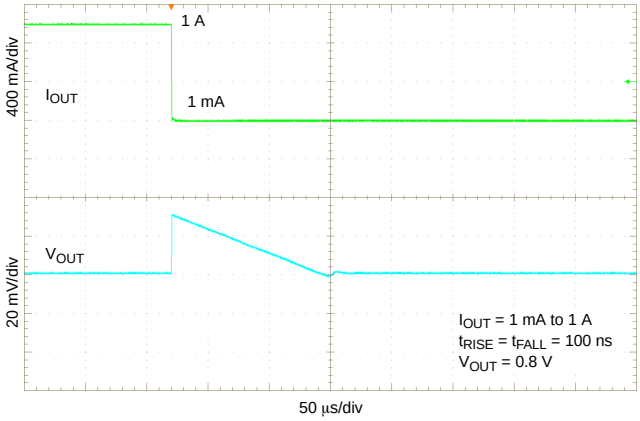


Figure 36. Load Transient Response − 1 A to 1 mA/100 ns

TYPICAL CHARACTERISTICS

(Conditions: V_{IN} = V_{OUT} + 100 mV, V_{BIAS} = V_{OUT} + 1.5 V, V_{EN} = V_{IN}, C_{IN} = 4.7 μF 0201 MLCC, C_{OUT} = 2x 4.7 μF 0201 MLCC, C_{BIAS} = 1 μF 0201 MLCC, unless otherwise noted)

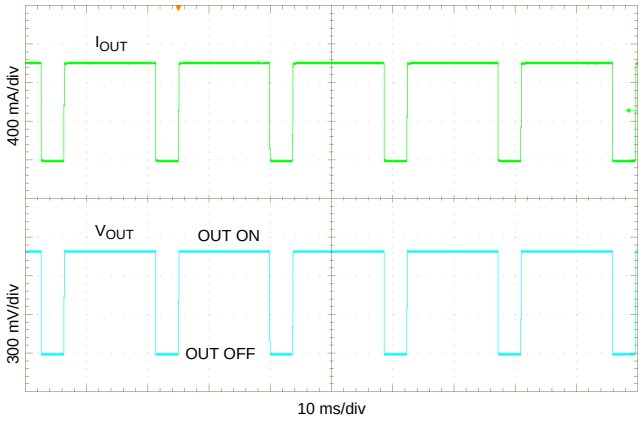


Figure 37. Thermal Shutdown (TSD) − Thermal Throttling

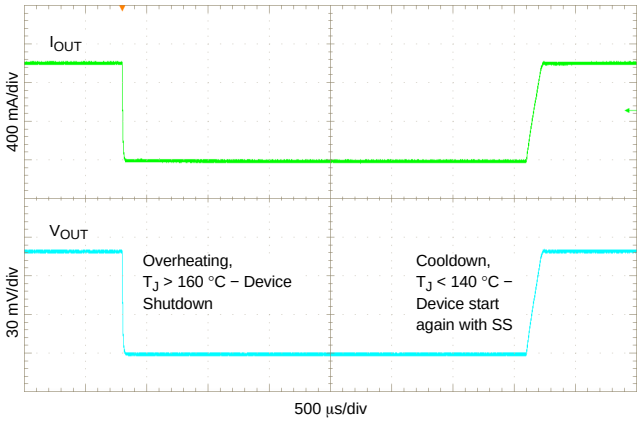


Figure 38. TSD Protection ON/OFF Detail

APPLICATION INFORMATION

The T30LMPSR131 is a next-generation dual-rail very-low-dropout voltage regulator featuring an NMOS pass device for output regulation from the V_{IN} input. The low-current internal control circuitry is powered by the V_{BIAS} supply.

The use of an NMOS pass transistor offers several advantages in applications. The very low V_{IN} to V_{OUT} voltage difference is the most important factor to use NMOS topology. It allows to increase efficiency, reduce power dissipation and heating. Separate BIAS voltage allows very low output voltages like 0.5 V with just 0.6 V power input voltage while maintaining excellent dynamic performance.

The T30LMPSR131 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis.

Dropout Voltage

Due to the presence of two independent supply inputs (V_{IN} and V_{BIAS}) and a single regulated output (V_{OUT}), the device specifies two distinct dropout voltages corresponding to each supply path.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} - V_{OUT}$) when V_{OUT} starts to decrease by percent specified in the Electrical Characteristics table. V_{BIAS} is high enough.

The second, the V_{BIAS} dropout ($V_{BIAS} - V_{OUT}$) is the state when internal NMOS gate driving voltage is not enough to open pass device more and V_{OUT} drops down to specified level. The both values are published in the Electrical Characteristics table.

Under Voltage Lock-Out (UVLO)

The device incorporates under voltage lockout protection (UVLO) on both inputs (IN and BIAS) to ensure safe start and shutdown when supply voltages rise or fall.

The BIAS UVLO threshold is set to approximately 2.1 V. When V_{BIAS} is below this threshold device is disabled even EN is asserted high. To prevent unwanted turn-on and off due to fluctuation BIAS supply rail hysteresis in UVLO block is set to 100 mV.

The IN UVLO threshold is set to approximately 80% of $V_{OUT(NOM)}$. When V_{IN} is below this threshold device is disabled even EN is asserted high. A 100 mV hysteresis is applied to avoid false turn-on/turn-off events caused by IN voltage fluctuations.

The soft-start feature is activated by both UVLOs. This ensures a well-defined startup profile across the full operating range and supports robust power-rail sequencing. When device is disabled by either UVLO condition, the active discharge (AD) is enabled and device the device enters a deterministic OFF sequence (valid only for options equipped by AD feature).

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are set to be compatible with 1.2 V I/O pins logic. The T30LMPSR131 can be easily used with all modern chipsets. If the enable function is not to be used, then the pin should be connected to V_{IN} or V_{BIAS}. If EN is connected to V_{IN} be careful about EN threshold.

If the EN pin voltage is < 0.325 V the device is guaranteed to be disabled. The pass transistor is turned off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active (devices with Output Active Discharge feature only) so that the output voltage V_{OUT} is pulled down to GND through a 150 Ω resistor. In the disable state the device consumes as low as typ. 0.5 μA from the V_{IN} and 0.5 μA from V_{BIAS}.

If the EN pin voltage is > 0.77 V the device is guaranteed to be enabled. The T30LMPSR131 regulates the output voltage and the active discharge transistor is turned off.

The EN pin has internal pull-down current source with typ. value of 0.3 μA which assures that the device is turned off when the EN pin is not connected.

Slew Rate Control

The device is optimized for camera sensor application and meets all requirements for using in modern camera applications such as a smartphones, cameras and image capture devices. Power supply specification of sensors often requires output voltage slew rate limitation to protect sensor during regulator start-up. The T30LMPSR131 incorporates soft-start feature which can assure smooth output voltage ramp without excessive inrush current and voltage undershoot. The device provides two options of slew rate speed, ‘Normal’ means typical rise time approx. 20 μs and ‘Slow’ option means rise time about 100 μs. More detail about star-up timing is specified in electrical table.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short. The device uses constant current limitation approach to protect against damage which means that output voltage drops down and output current keeps similar level specified by parameter I_{CL} in Electrical characteristic. The I_{CL} value is defined when V_{OUT} falls down to 90% nominal output voltage.

Thermal Protection

When the die temperature exceeds the Thermal Shutdown threshold (TSD − 160 °C typical), Thermal Shutdown event is detected and output voltage is turned-off, immediately.

Once the device temperature falls below the 140 °C regulator is turned-on again. The soft start feature is

activated when output voltage is turned-on after TSD event. The internal built in hysteresis prevents excessive output OFF and ON switching and provides additional time to die cooling.

The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipation in the device increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affects the rate of junction temperature rising for the part.

The maximum power dissipation the device can handle is given by:

$$P_{D(MAX)} = \frac{125\ ^\circ C - T_A}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the device for given application conditions can be calculated from the following equation:

$$P_D = \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} + V_{BIAS} \cdot I_{GND} \quad \text{(eq. 2)}$$

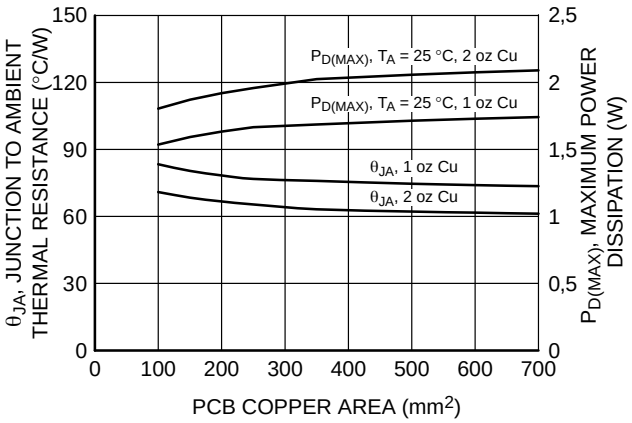


Figure 39. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area

Reverse Current

The NMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The T30LMPSR131 is very fast device which features very good Power Supply Rejection ratio even with very small $V_{IN} - V_{OUT}$ headroom. The lowering headroom, real input voltage must be watched carefully to avoid regulator drop out and performance degradation. If desired the PSRR at higher frequencies in the range 1 MHz − 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Input Capacitor Selection (C_{IN})

It is recommended to connect at least a 4.7 μF Ceramic X5R or X7R capacitor as close as possible to the IN pin of the device. Larger input capacitor may be necessary if fast and large load transients are encountered in the application. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. or max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Bias Capacitor Selection (C_{BIAS})

The bias pin provides supply voltage for internal circuitry and could affect device performance. The 1 μF decoupling capacitor should be connected as close as possible to BIAS pin to provide low impedance path for unwanted AC signal coupled on bias line. The BIAS capacitor also provides stable voltage for internal reference and regulation loop which improve device performance. The X7R or X5R ceramic capacitor are recommended for their reliable performance over wide temperature range.

Output Decoupling Capacitors (C_{OUT})

The T30LMPSR131 is designed to achieve the best-in-class dynamic response. It brings some specific requirements to output capacitor selection. The only quality X7R, X5R and better ceramics capacitors should be used.

The T30LMPSR131 is fully stable over all conditions with effective capacitance at least 2.2 μF. The device is ideal for space-constrained PCB designs, where its compact package combined with 0201-size capacitors enables maximum board space efficiency.

Capacitors of this size have significant capacitance DC-derating. This fact should be kept in mind in output capacitor selection. The Figure 40 shows capacitance derating for three different package size.

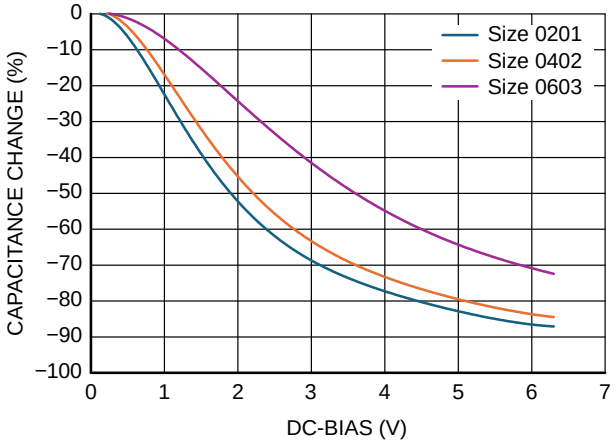


Figure 40. Capacitance Change vs. DC Voltage Applied

Capacitance change is also depended on capacitor thickness. For applications where small PCB area is limitation but height is not critical the thicker capacitor with same footprint provides better effective capacitance.

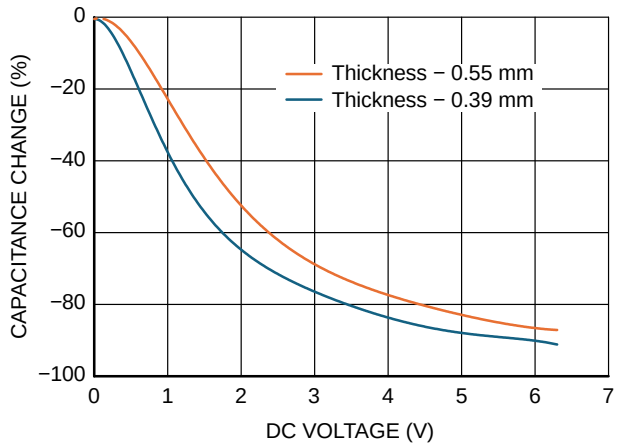


Figure 41. Capacitance Change vs. Caps Package Thickness

The device is not sensitive to high total output capacitance and can handle capacity up to 47 μF. The T30LMPSR131 can also handle additional capacitors spread over board with no physical dimension limitation.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics output capacitors should be placed as closed as possible to output pin. The T30LMPSR131 includes dedicated SNS pin which should be connected directly to output capacitors to keep device stable and high performance. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). The Figure 42 shows recommended PCB layout.

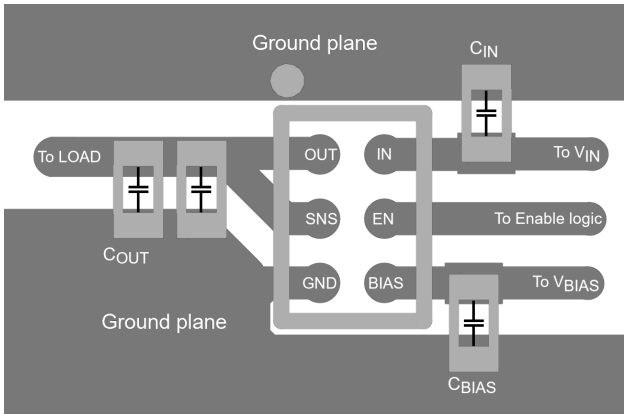


Figure 42. Recommended PCB Layout

To increase application efficiency as small as possible $V_{IN} - V_{OUT}$ headroom is desirable. It is necessary to be very careful in PCB design because any additional PCB resistance between LDO power source and input pin causes voltage drop which further reduces voltage headroom. For example: If V_{OUT} = 800 mV, V_{IN} = 900 mV and peak current 500 mA. Then 20 mΩ path resistance between LDO power source (for example DC-DC) output and LDO input cause voltage drop 10 mV. It means, we reduced usable headroom to 90 mV from total 100 mV budget. If we subtract maximum dropout 50 mV only 40 mV left for correct LDO operation. When we take into account 1% LDO accuracy then the headroom is reduced to only 32 mV. In the example, DC-DC output voltage accuracy is not take into account and LDO voltage headroom is further reduced.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Option	Package	Shipping†
T30LMPSR131CFCT080T2G	0.80 V	DQ	Output Active Discharge, Slow Turn-On Slew Rate	WLCSP6 Case 567YX (Pb-Free) UBM: 240 μm Bump Type: (98.2% Sn/1.8% Ag) Plate	10,000 / Tape & Reel
T30LMPSR131CFCT090T2G	0.90 V	DP			
T30LMPSR131CFCT100T2G	1.00 V	DR			
T30LMPSR131CFCT120T2G	1.20 V	DT			
T30LMPSR131CFCT180T2G	1.80 V	DU			

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

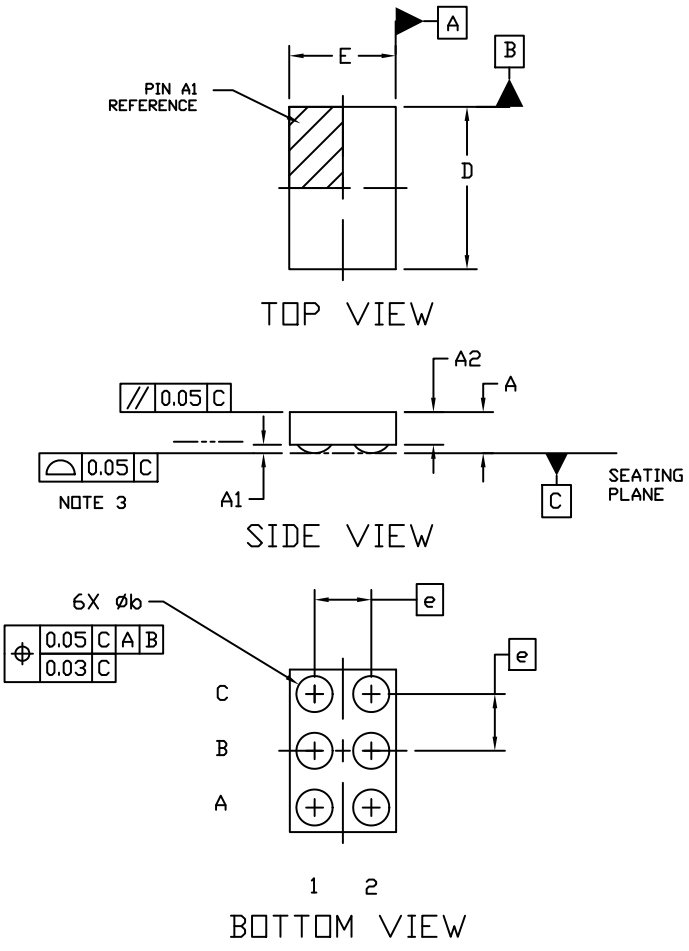
8. To order other package and voltage variants, please contact your **onsemi** sales representative.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	3/24/2026

WLCSP6 1.145x0.75x0.33
CASE 567YX
ISSUE O

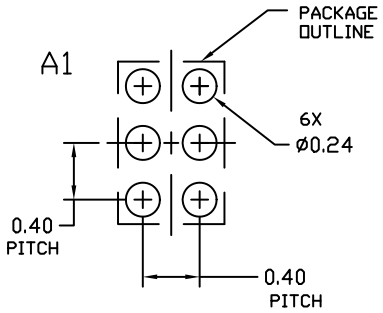
DATE 29 JAN 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

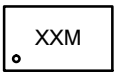
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	0.33
A1	0.04	0.06	0.08
A2	0.230 REF		
b	0.220	0.240	0.260
D	1.095	1.145	1.195
E	0.700	0.750	0.800
e	0.400 BSC		



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP6 1.145x0.75x0.33**	**PAGE 1 OF 1**

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